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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BAUER, SCOTT ALLEN	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

Office Action Summary	Application No.	Applicant(s)	
	10/707,963	ANAND ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13 and 18-20* is/are rejected.

7)☒ Claim(s) *12 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because Figures 4 & 5 are misnumbered. In the applicant's specification, Figure 4 discloses a fuse latch circuit, and Figure 5 discloses a Reference Generator. However, in the drawings, Figure 4 discloses the Reference Generator, and Figure 5 discloses the latch circuit. The heading "Figure 5" should be changed to read "Figure 4", and the heading "Figure 4" should be changed to read "Figure 5". Alternately, the specification should be changed to accurately reflect the drawings.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the band gap current reference of Claim 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

In paragraph 00027, the disclosure reads, "[T]he voltage on input node (FT) ***112*** will be BELOW the latch –voltage". The line should be changed to read, "[T]he voltage on input node (FT) ***122*** will be BELOW the latch –voltage".

In paragraph 0029, the disclosure reads, "the L1 latch in 103 must switch as an ***interter*** – not as a latch". The line should be changed to read the L1 latch in 103 must switch as an ***inverter*** – not as a latch".

In paragraph 0032, the disclosure reads, "The (VSWITCH) 106 current reference is created by Reference Current Generator ***20*** in Fig. 5". The line should be changed to read, "The (VSWITCH) 106 current reference is created by Reference Current Generator ***200*** in Fig. 5 ". Appropriate correction is required.

4. The disclosure is objected to, as there is no support for the claimed band gap current reference of Claim13.

Claim Objections

5. Claim 6 recites the limitation "said fuse element" in line 1. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 13 claims invention of a trip point current reference comprising a band gap current reference. However, the disclosure never teaches a device called a band gap current reference. As best understood by the examiner, the band gap current reference will be interpreted as a resistor selection block (Fig.4, 201), for the purposes of the prior art rejection.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 18 rejected under 35 U.S.C. 102(b) as being anticipated by Bertin et al. (US 6384666).

9. With regard to Claim 18, Bertin et al. discloses a latch device (90) having a variable resistive trip point comprising: a voltage source (V_{int}), an adjustable trip point current source (vITRIP), a latch circuit (90) having a fuse latch a trip point control means (74) to control the current passing through the latch circuit, a compensation means for adjusting the trip point current reference (30), and a means for compensating the

current reference for changes in process, voltage or temperature to maintain a constant resistive trip point. (column 4, lines 20-67 & column 5 lines 1-34).

Bertin et al. discloses that the resistance of an anti-fuse can change over time with stress from process, temperature and voltage. The trip point current reference (30), compensates for this by changing the reference current to maintain the proper trip point, as taught in column 4, lines 20-67 & column 5 lines 1-34.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 11, 19 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingalls (US 5892716) in view of Frary et al. (US 5289412).

12. With regard to Claim 1, Ingalls in Figure 4a teaches a latch device (120) that has a variable resistive trip point (column 5 lines 14-16). The latch contains a voltage source (Vcc), an adjustable trip point current reference (124 &128), a latch circuit having a fuse latch output (123), and a trip point control element that operates to control the

amount of current passing through the latch circuit based on the adjustable trip point current reference (column 6 lines 11-19).

Ingalls does not teach a latch device circuit where a latch mimic circuit compensates the current reference.

Frary et al., in Figure 1, teaches circuitry for checking the condition of a memory cell, which is a latch circuit, where a mimic circuit is used for compensation. Column 3 lines 66-68 and column 4 lines 1-4 teach that a FET (20) is placed in line with a terminal of a difference amplifier (14) for the purpose of matching the impedance of the select FET (15), on the opposite side of the differential amplifier.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls with Frary et al. by placing a device matching the impedance of the latch circuit (123) in series with the current reference (121) with the latch circuit (123) for the purpose of providing very reliable, high performance sensing operations as stated in Frary et al. (column 1 lines 25-31).

13. With regard to Claim 11, Ingalls, in Figure 4, further discloses a latch circuit with a polling transistor (144), the gate being connected to a strobe signal (RDFUS*), which polls the condition of the fuse (112) when the strobe signal input is in an active state (column 6 lines 65-67 & column 7 lines 1 & 2).

14. With regard to Claim 13, Kanno, in Figure 3, further discloses the band gap current reference (2 & 3). This is based on the examiners assumption that the disclosed band gap current reference is the resistor selection block of Fig. 4.

15. With regard to Claim 19, Ingalls, In figure 3, teaches a method to control a variable resistive trip point fuse latch having a plurality of fuse elements (112) with differing states comprising: determining the state of the fuse elements (column 1 line 43-45), storing the state of the fuse elements (column 1 lines 45-49), selecting a predetermined fuse element, and comparing the fuse resistance to the trip point current reference (column 3 lines 7-12).

Ingalls does not teach a latch device circuit where a latch mimic circuit compensates the current reference.

Frary et al., in Figure 1, teaches circuitry for checking the condition of a memory cell, which is a latch circuit, where a mimic circuit is used for compensation. Column 3 lines 66-68 and column 4 lines 1-4 teach that a FET (20) is placed in line with a terminal of a difference amplifier (14) for the purpose of matching the impedance of the select FET (15), on the opposite side of the differential amplifier.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls with Frary et al. by placing a device matching the impedance of the latch circuit (123) in series with the current reference (121) with the latch circuit (123) for the purpose of providing very reliable, high performance sensing operations as stated in Frary et al. (column 1 lines 25-31).

16. With regard to Claim 20, Ingalls in view of Frary et al. discloses the method of Claim 19 as described above. Frary et al. further teaches a method of circuit compensation where the mimic circuit is compensated in changes in variation in processing, temperature, ands supply voltage (column 1, lines 25-31).

17. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingalls in view of Frary et al. and further in view in Kanno (6377113).

18. With regard to Claims 2 & 3, Ingalls in view of Frary et al. teaches the device as outlined above in Claim 1. Ingalls further teaches that the trip point control element is a transistor (122) and that the source is connected to the voltage source.

Ingalls in view of Frary et al. does not teach that the gate of the trip point control transistor is connected to the trip point current reference or that the drain of the transistor is connected to the latch circuit.

Kanno, in Figure 3, teaches reference current generating circuit with a variable trip point. Kanno further teaches a trip point control element (6) with a gate connected to the adjustable current reference and with a drain connected to an output which could be a latch. This configuration allows a change in the trip point reference to change the current (Iref) flowing through control FET (6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls in view of Frary et al. with

Kanno for the purpose of providing reference current suitable for being placed in a MOS semiconductor IC, capable of generating a precise reference current without being influenced by variation of transistor threshold voltages and temperature changes as stated by Kanno (column 2 lines 10-15).

19. With regard to Claim 4-6, Ingalls in view of Frary teaches the latch device as set forth in Claim 1. Ingalls further teaches that the fuse element being tested is an antifuse, and that a mimic circuit can receive a reference current prior to being used to test the antifuse resistance.

Ingalls in view of Frary et al. does not teach a feed back circuit used to determine the reference current that will make the latch input voltage equal to the latch-inverter trip point, and that the latch voltage is monitored by a differential amplifier.

Kanno, in Figure 3, teaches a feedback circuit (9) that is a differential amplifier, which outputs an intermediate voltage. This voltage establishes the reference current based on an offset voltage, which can be input from the latch voltage (column 4 lines 19-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls in view of Frary et al. with Kanno for the purpose of stabilizing the reference voltage to an off-set voltage (column 4 lines 19-36).

20. With regard to Claims 7-9, Ingalls in view of Frary teaches the latch device as set forth in Claim 1.

Ingalls in view of Frary does not teach that the adjustable current trip point reference that is adjusted binarily.

Kanno, in Figure 3, teaches a trip point current reference (1), which has a plurality of selectable inputs (TRM1 & TRM2), connected to binarily weighted reference transistors (10A-F), which are operated and adjusted binarily to change the adjustable trip point current reference (column 4 lines 55-67 & column 5 lines 1-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls in view of Frary with Kanno for the purpose of providing a reference current generating circuit can be realized, which is capable of supplying a reference current having a high precision and a high stability in relation to a variation the threshold voltage of the FET, caused by variation in the manufacturing process and a temperature change (column 2 lines 38-43).

21. With regard to Claim 10, Ingalls in view of Frary et al. teaches the latch device as set forth in Claim 1.

Ingalls in view of Frary et al. does not teach the use of a current mirror control in the trip point current reference.

Kanno, in Figure 3, teaches the use of a current mirror in a current reference generator to supply a reference current to a device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ingalls in view of Frary et al. with Kanno for the purpose of supplying a constant reference current to the latch regardless of the latch resistance.

Allowable Subject Matter

22. Claims 12 & 14-17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. Claim 12 would be allowable if rewritten in independent form because the prior art does not teach that the trip point reference generator is adjusted to allow a maximum amount of current to pass from a voltage source into a latch circuit when the strobe signal, input to a bypass transistor in the current reference generator, is in an inactive state.

24. Claim 14 would be allowable if rewritten in independent form because the prior art does not teach that the trip point reference is operated to provide three different trip points. Ingalls teaches that two different trip points can be set for testing the resistance margin of a fuse element, and for normal operation. However, the prior art does not

teach a third trip point set for improving soft-error immunity by disabling the current reference generator.

25. Claim 15 would be allowable if rewritten in independent form because the prior art does not teach the use of a buffer such as an inverter to prevent creep-up of the feed-back transistors. Ingalls (US 5978297) teaches a circuit for strobing an antifuse circuit where a latch (192) is buffered by an inverter (198). However, the buffer is placed in the circuit after the feedback transistors and so it does not prevent creep-up.

26. Claims 16 & 17 would be allowable if rewritten in independent form because they are dependant on Claim 15, which would also be allowable if rewritten in independent form.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB

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PRIMARY EXAMINER